APPLICATION NOTE

TDA8761 /TDA8762 / TDA8762A
EVALUATION BOARD DOCUMENTATION

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Summary

This note describes a demonstration board which facilitates the evaluation of the TDA8762(A) 10 bit analog to digital converters and the TDA8761 9 bit analog to digital converter (sections 2, 3, 4, 10, 11).
In addition the functioning of the TDA8762(A) is shortly described (sections 1, 5, 7, 8) and several methods to provide input offset and top and bottom references are shown (sections 5, 6).

CONTENTS

1. INTRODUCTION

TDA8761, TDA8762 and TDA8762A are high speed, low power, pin to pin compatible, analog to digital converters.

They have been designed for professional applications : video data digitizing, medical imaging, ΣΔ modulators, cable TV, Digital Video Broadcasting (DVB) ...

Mains features of these ADCs, which are derived from the same ADC core, are shown in the following table:

	Resolution (bit)	Full Scale Bandwidth (MHz)	Power (mW)	Sampling Frequency (MSPS)
TDA8761	9	40	360	30
TDA8762	10	40	380	40
TDA8762A	10	40	380	60 (/6) 80 (/8)

The effective number of bits, when a full scale sinewave input is applied, stay above 9 bits for a signal frequency as high as 12.5 MHz. Digitizing of 20 MHz full scale square wave signals (shape of CCD output signals) with the 10 bit resolution is possible if the settling time (typ 2,5 ns) and the signal slope (max 400 V/µs) are respected.
There are still 8 effective bits (10 bit ADCs) when a 20 MHz full scale sinewave is digitized.
The linearity performance of these ADCs ensures the 9 bit version the required conversion accuracy in case of 256QAM demodulator.
Because of their high analog bandwidth, a Sample & Hold is generally not required in front of the ADC analog input.
This ADC architecture allows a conversion time of only one clock cycle. In addition there is no restriction in using very low clock frequencies.

Application requires few external components and is similar for TDA8761, TDA8762 and TDA8762A versions. Consequently this note applies for the three converters.

TDA8762 package is a plastic shrink small outline package SSOP28 (SOT341-1).

The present demonstration board intends to facilitate an evaluation of the main TDA8762, TDA8762A, TDA8761 characteristics. It is realized with a three layers PCB with one internal ground plane. The following features are included :

⇒ On board quartz oscillator or a connection for an external clock. For ADC characteristic measurements a clock generator with a very low jitter should be used (see section 7).

⇒ ADC voltage references and ADC 5V supplies are derived from a 8V supply by the means of voltage regulators.

⇒ Connectors allow external voltage references & external output supply (VCCO).

⇒ DC or AC input signals are allowed. The input offset can be provided in three different ways :

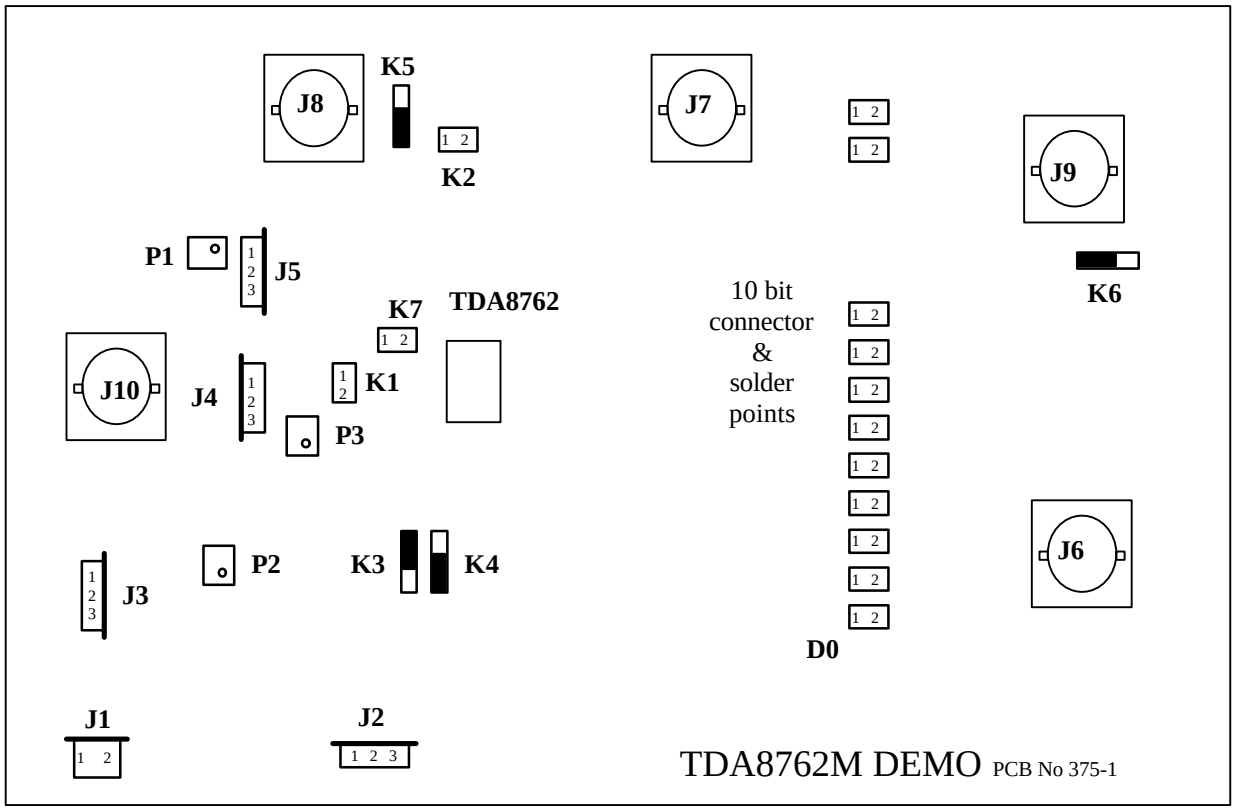
* by a resistor bridge,
* by a resistor connected to the middle reference voltage (pin 7),
* by an external voltage source.

⇒ A 10 bits D/A converter has been added on the board to verify the properoperation of the ADC with an oscilloscope.

The performances of the D/A converter are not as high as those of the A/D converter.
Consequently the on-board D/A converter cannot be used for a correct study of the ADC characteristics.

WARNING : The on-board D/A converter does not withstand a low output load, so it is necessary to check the strobe/scope input impedance before connection.

2. CONNECTOR, SWITCH AND JUMPER POSITIONS



3. CONNECTOR, SWITCH AND JUMPER LIST

Reference	Type	Function
J1	2 point connector	Board supply (8V)
J2	3 point connector/jumper	Internal/external VCCO supply selection J2.1, Ground. J2.2,VCCO-ext: External input for VCCO. Must be connected with J2.3 if the internal VCCO is selected. An LC filter is provided between the J2.2 connector pin and the TDA8762M VCCO pin 28 & 13. J2.3, on board +5V for VCCO
J3	3 point connector/jumper	Internal/external top reference selection: J3.1, Ground J3.2, On-board adjustable top voltage reference J3.3, VTOP-ext: Pin for external top voltage reference connection, must be connected with J3.2 if internal top voltage reference is used.
J4	3 point connector/jumper	Internal offset (provided by VMED)/external input offset selection J4.1, Ground. J4.2, VMED: Vmedium voltage reference. Vmedium (tda8762 pin 7) can be use to provide input offset (If it is well decoupled from the input signal by a RC cell). In that case J4.3 and J4.2 must be connected. J4.3, IN-DC: This pin allows DC input connection or external input offset.
J5	3 point connector/jumper	Internal/external bottom reference selection: J5.1,VBOT-ext: Pin for external bottom voltage reference connection. J5.2,VBOT: Resistive load (1K potentiometer and 68Ω in parallel) must be connected with J5.1 if internal bottom voltage reference is used. J5.3,Ground
J6	BNC	DAC output (high impedance probe is necessary)
J7	BNC	In range output (digital TTL output)
J8	BNC	ADC (or ADC+DAC) clock input (50 Ω input)

Reference	Type	Function
J9	BNC	DAC clock input (50 Ω input)
J10	BNC	Signal input (50 Ω input)
K1	2 point jumper	Internal offset (provided by a resistor bridge) connection

		A resistor bridge (P3;R4;R9;C37) can be used to provide the input offset. In that case K1 must be connected. This resistor bridge is supplied by the top voltage reference.
K2	2 point jumper	Clock test point
K3	switch	Two complement (pin 2) control Upper position TC=1 (binary output) Lower position TC=0 (two complement output)
K4	switch	Output Enable control Upper position OE=1 (Output high impedance) Lower position OE=0 (Output enabled)
K5	switch	External/internal ADC clock selection Lower position : internal clock selected Upper position : external clock selected (J8 connector)
K6	switch	Internal/external clock selection for the DAC Left position : internal clock selected Right position : external clock selected (J9 connector)
K7	2 point jumper	Not used,must stay connected

4. INITIAL SETTINGS : AC INPUT, ON BOARD QUARTZ OSCILLATOR, 3.8 V & 1.3 V VOLTAGE REFERENCES

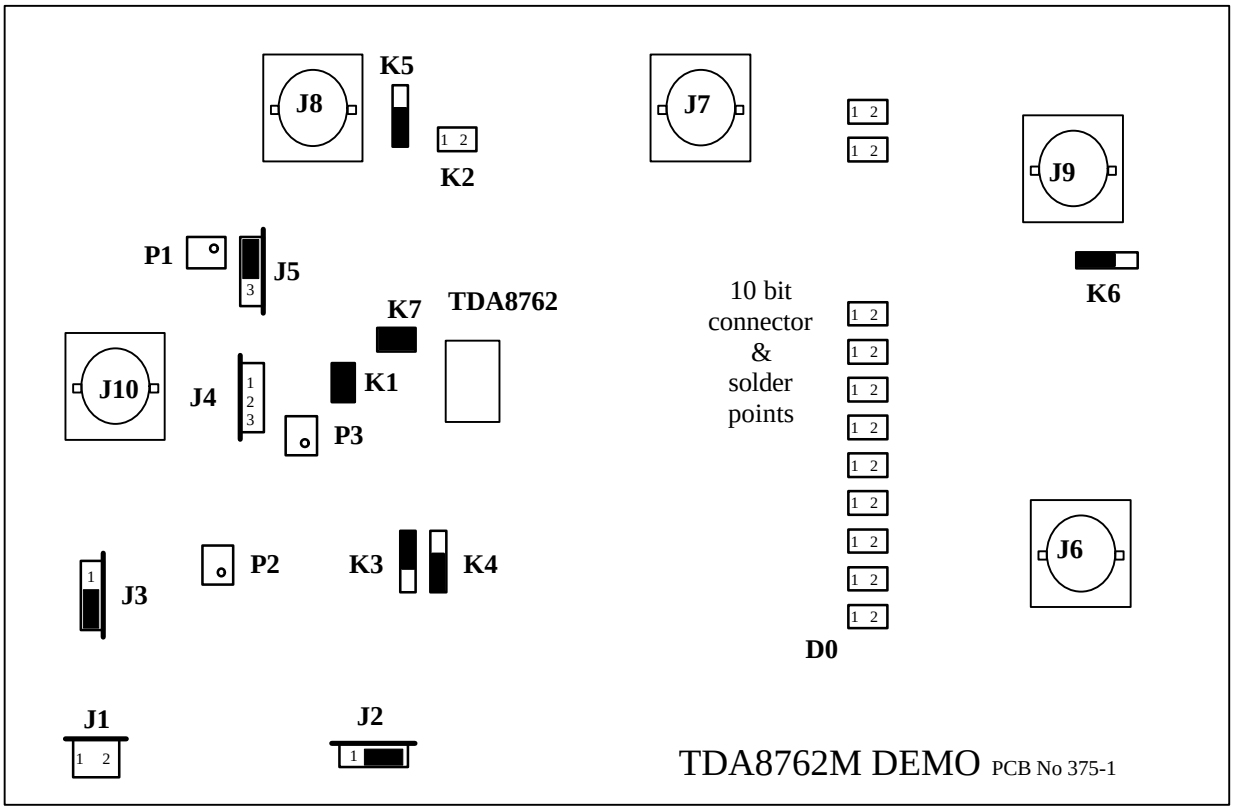
The board supply must be set at 8 V.

All the supplies (ADC, DAC) are derived from a 7805 regulator and are well decoupled from each othersby the means of LC filters. In this configuration the AC signal source must be provided by an external generator which is connected to the board by the J10 connector (dynamic input impedance is 50 Ω).

The ADC top voltage reference is provided by an on-board adjustable regulator (TL431) and it is well decoupled by an LC filter. The ADC bottom voltage reference is simply set by a resistive load made up of a potentiometer (P1) and a resistor (R1) in parallel.

The input offset is derived from the ADC top voltage reference and is made up of a resistor bridge (P3;R4;R9;C37).

To obtain this operational mode, jumpers, switches are set as shown in the following figure :



Potentiometers P1, P2, P3 are adjusted as explained in the following :

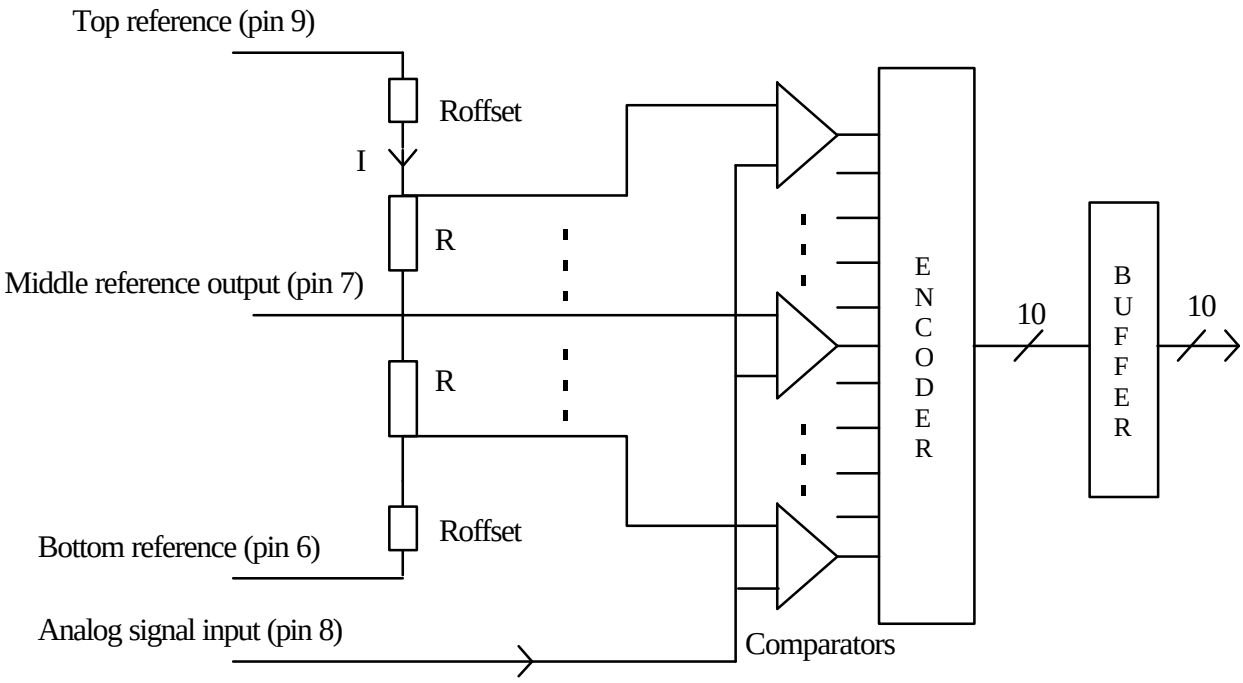
P2 is used to adjust the output voltage of the on-board adjustable regulator (IC3). This regulator provides both : the ADC top voltage reference and the supply for the input offset.
P2 is adjusted around 244 Ω in order to obtain 3.8 V at the adjustable regulator output.

P1 allows the adjustment of the bottom voltage reference. In order to obtain a bottom reference of 1,3 V, P1 is adjusted around 120Ω.

P3 allows the adjustment of the input offset. In order to obtain an input offset of 2.55 V, P3 is adjusted around 1990Ω ; therefore the dynamic input impedance of the analog signal input (J10 connector) is given by R9 (50Ω) and R4 (1KΩ) in parallel and is equal to 48Ω.

5. VOLTAGE REFERENCES

Here is a block diagram which explains the TDA8762 working:



During the A to D conversion the analog input signal (pin 8) is compared to voltage references by using of voltage comparators (in fact these comparators are folding amplifiers).

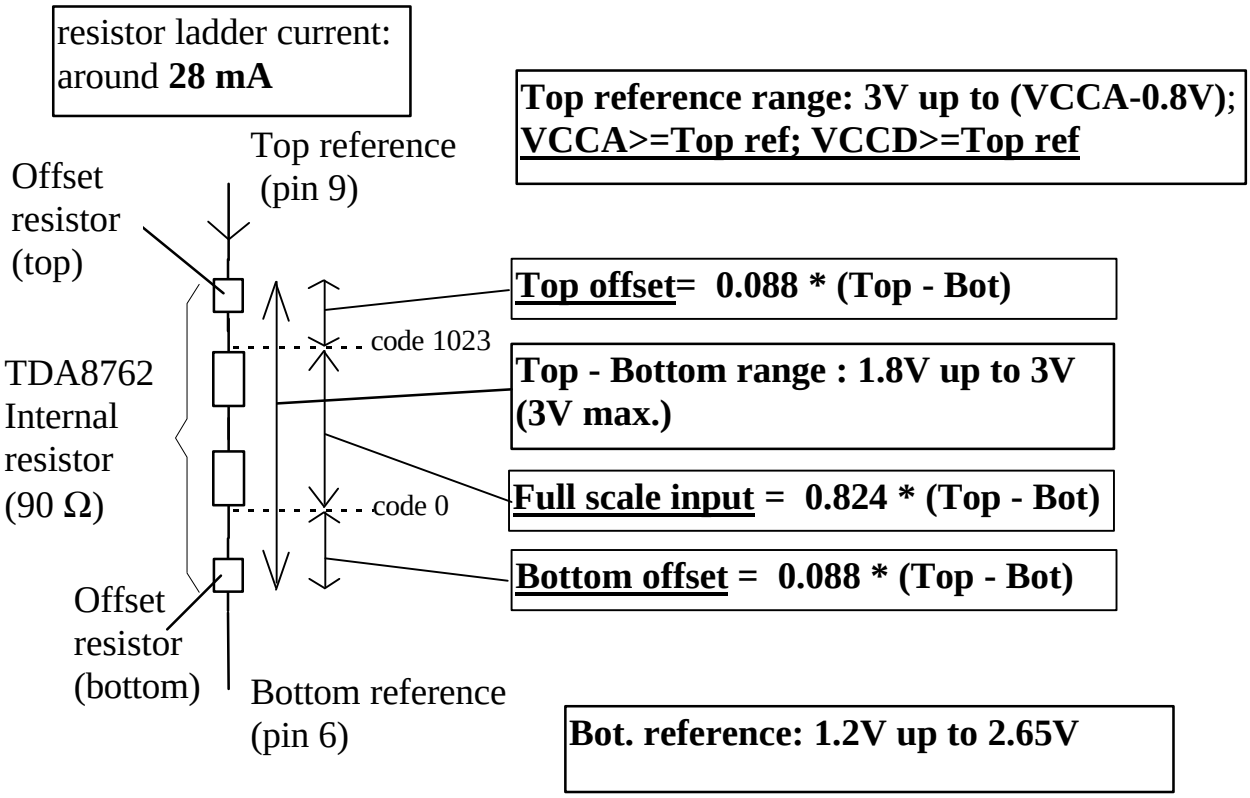
The full scale analog signal input range (FS) is given by:
FS= 0.824 (Top ref. - Bottom ref.) ; The 0.824 coefficient is due to the two offset resistors.

The comparator's voltage references are derived from a resistor ladder which is supplied through Vtop (pin 9) and Vbottom (pin 6). Therefore if the Vtop and Vbottom are not well regulated the A to D conversion will be affected.

Top reference (pin 9) is the highest voltage reference. Bottom reference (pin 6) is the lowest voltage reference. Consequently a current I is flowing from pin 9 to pin 6.

The typical value for the internal resistor ladder is 90 Ω at 25°C.

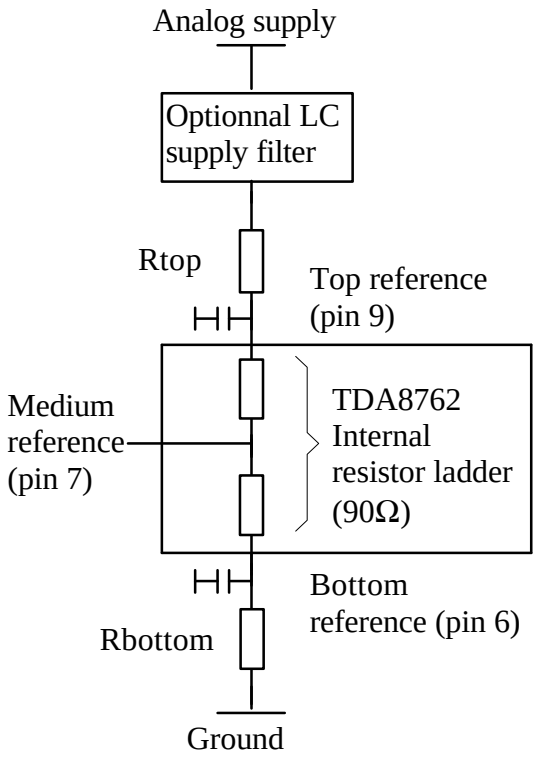
As shown in the following schematic the TDA8762 (TDA8762A, TDA8761) is versatile regarding the choice of the top and bottom voltage references. Therefore it is possible to find top and bottom voltage references which the fit with majority of the applications.



Regulation of the Vtop & Vbottom voltage references depends on the level of cost and quality which are required by the customer application.
Several methods providing these voltage references are shown in this section.

5.1 TOP & BOTTOM REFERENCES DERIVED FROM THE ANALOG SUPPLY

If the analog supply is well regulated a simple resistor bridge will be efficient (see following figure).



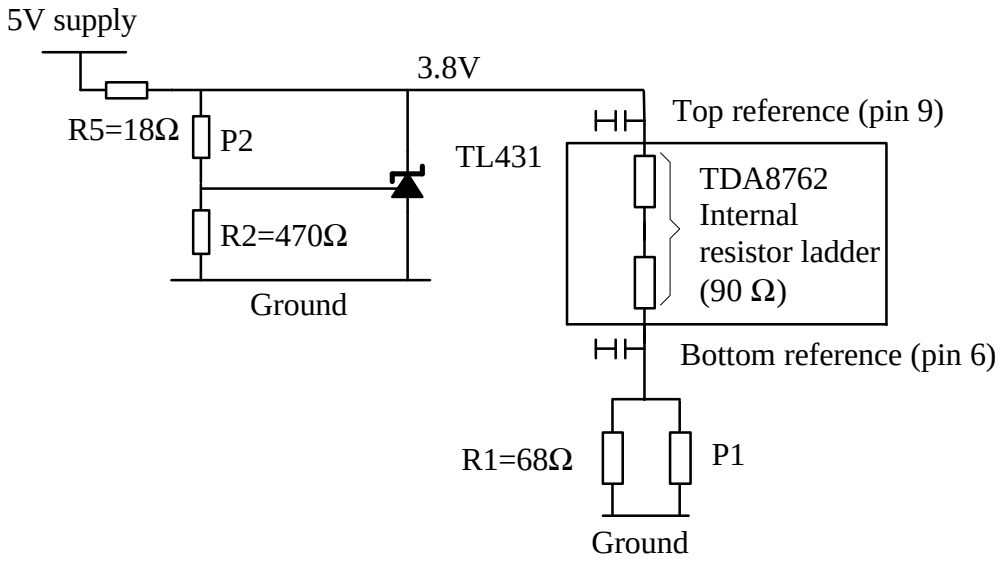
An optional filter can be added on the analog supply (depending on supply noise level).

Typical voltages for a 5V analog supply operation are 3.8V for top reference and 1.3V for bottom reference . The current flowing through the 90 Ω resistor ladder is 28 mA ;

Rtop = 43.2 Ω
Rbot = 46.8 Ω
Remarks: Here, the spreads due to process and temperature are not taken into account.

5.2 TOP & BOTTOM REFERENCES DERIVED FROM REFERENCE VOLTAGE REGULATOR(S)

In some cases (noise on supply, several ADC's mounted in parallel ...) solutions with precision regulators (Philips µA723, Texas Inst. TL431,...) may be prefered.
On this board a regulator (IC3, TL431) is used to provide the top reference whereas the bottom reference is simply made up of an adjustable resistive load (P1 & R1 in parallel). It is possible to adjust, respectively, the top and bottom voltage value with the P2 and P1 potentiometers.



The voltage value of the top reference is given by the following formula :

$$Vtop = 2,5\ (1 + \frac{P2}{R2})$$

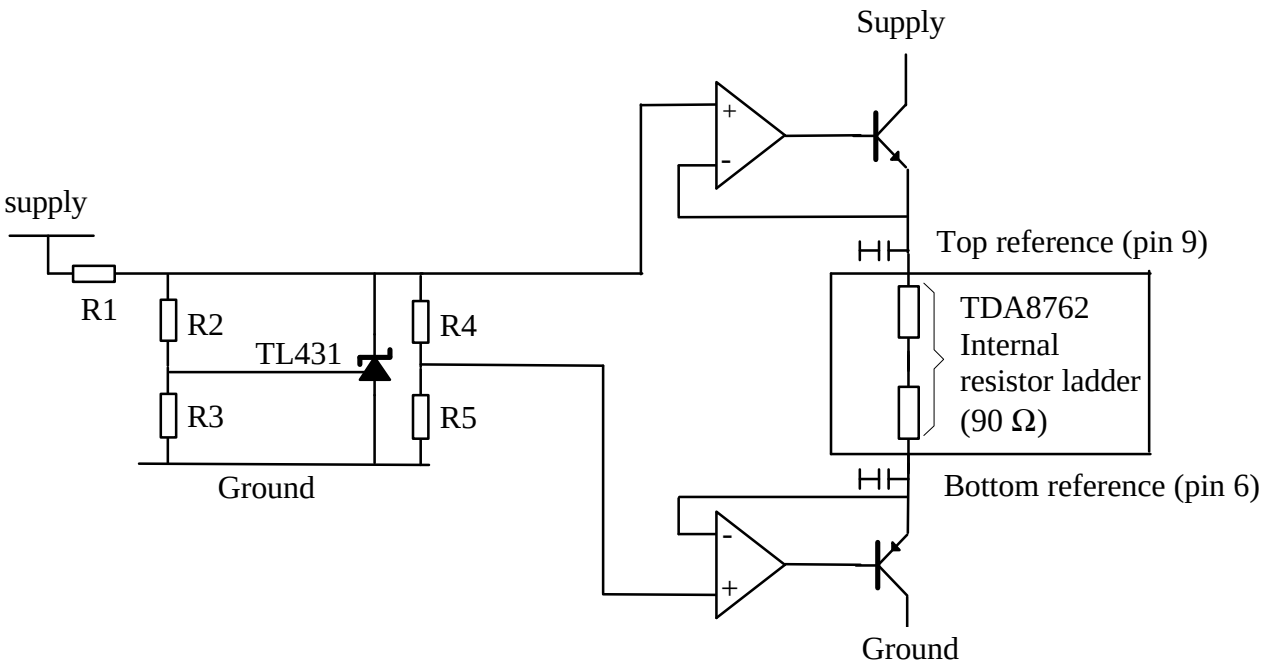
The voltage value of the bottom reference is given by :

$$Vbot = Vtop\ (x\ \frac{Rbot}{Rbot + Rladder})$$

where $Rbot = \frac{R1P1}{R1 + P1}$ and Rladder is the ADC internal ladder resistor (around 90 Ω).

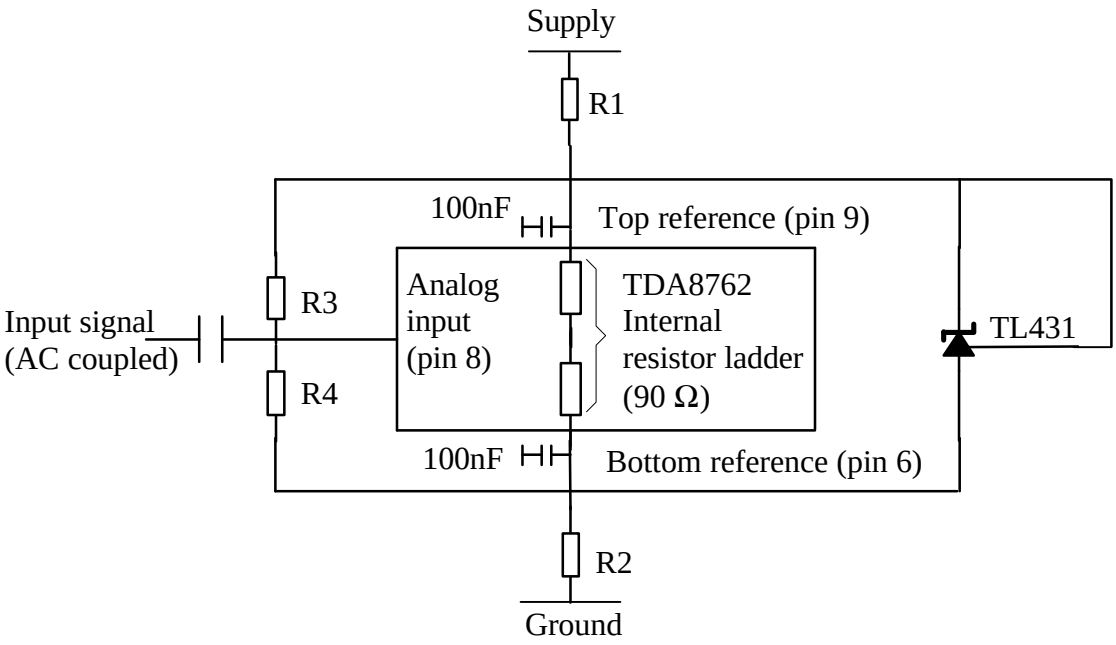
It is also possible to connect external voltage references with two connectors, J3 (for the top reference) and J5 (for the bottom reference).

If several ADC are mounted in parallel or if a very high precision of the voltage references over the whole temperature range is required, the following schematic can be used :



The transistor type depends on the number of TDA8762 mounted in parallel. A 28 mA current (typ) is required for each TDA8762.
If only one ADC is used the operational amplifier and the transistor which drive the top reference can be skipped. In this case the voltage regulator controls directly the top reference.

In the following electrical diagram, top and bottom references are regulated by only one component (TL431):



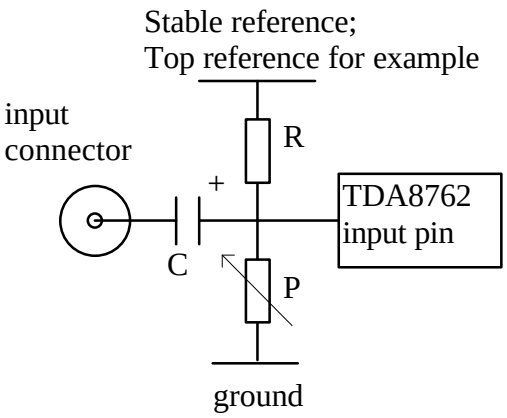
The (top - bottom) difference is set at 2.5V by the TL431, so the full scale input is set at 0.824*2.5=2.06V. In addition the input offset is set at (Vtop+Vbottom)/2 by two equal resistors (R3 and R4).
In this case the TL431 maintains the (top - bottom) difference at 2.5V over temperature and supply variations. Because the input offset is derived from the top and bottom references, it is also regulated at (Vtop+Vbottom)/2 over the temperature and supply variations.
Typical resistor values for a 5V application and for one TDA8762 are:
R3=R4=2.2KΩ, R1=R2=25Ω. The current flowing trough the R1, R2 resistors is around 50 mA (The TL431 requires a minimum current to provide proper regulation).

6. INPUT OFFSET

When AC coupling is used with the TDA8762 it is necessary to provide an input offset in order to respect the TDA8762 full scale input range.
Relations between the Vtop reference,the Vbottom reference, the maximum amplitude of the analog signal and the input offset are:
Max. amplitude of analog signal is (Vtop-Vbot)*0.824 and the input signal is centered around the input offset which is (Vtop+Vbottom)/2.
Consequently, if Vtop=3.8V and if Vbottom=1.3V the maximum amplitude of the analog signal is 2.06V and the input offset is 2.55V; code 0 is obtained for a 1.52V input, and code 1023 is obtained for a 3.58V input.

Input offset can be provided by many different methods. Several methods are explained in this section.

6.1 INPUT OFFSET DERIVED FROM A RESISTOR BRIDGE



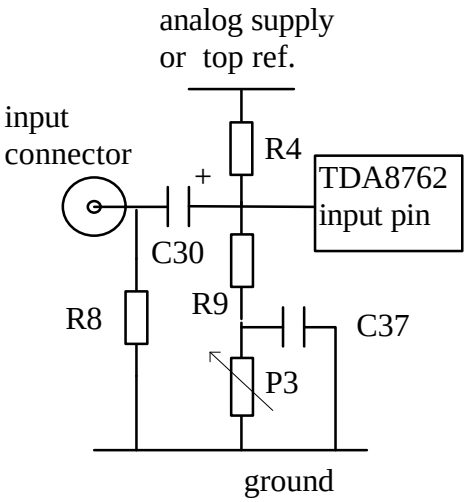
When a resistor bridge is used to provide an offset the current flowing through the resistors must be at least 10 times greater than the signal current (TDA8762 analog input current is 0 to 70µA) in order to guarantee the stability of the input offset. Consequently the resistive value of this resistor string must be below 5.5KΩ (with a 3.8V top reference).

If the input signal generator used to test the TDA8762 requires a 50Ω load, R must be set at 74.51Ω and P at 152Ω (Vtop=3.8V,Vbottom=1.3V, Input offset=2.55V), in order that the dynamic impedance (R & P in parallel) be 50Ω.

Remarks:

This method provides a correct input offset but the current flowing through the resistor bridge is high: 16.7mA (R=75Ω, P=152Ω and top reference=3.8V).

In order to reduce this current consumption another method is used on board, but it requires two more components (one capacitor and one resistor):



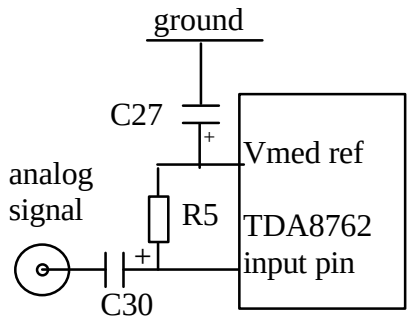
R9 is equal to the output load of the external signal generator. C37 allows ground connection between R9 and P3 in dynamic mode. Typical values when a 50 Ω signal generator is used are: R4=1KΩ, R9=50Ω, P3=5KΩ (set at 1990Ω), C37=100nF, then the current flowing through the resistor bridge is only 1.25mA with a 3.8V supply.
The solder print of an optional resistor R8 is provided in order to allow other impedance adaptations.

→ When it is possible, it is better to replace the potentiometers by fixed resistors. This will avoid possible distortion effects on the input signal due to the capacitive components of the potentiometers.

→ It can be difficult to obtain the exact output load and the exact input offset when they are made up of fixed resistors, because the accuracy of the resistors is limited. Furthermore the resistor values change with temperature. Consequently in some professional applications it is better to provide the correct load and the correct input offset with operational amplifiers.

6.2 INPUT OFFSET DERIVED FROM THE MEDIUM REFERENCE

In this case the input pin is connected to the medium voltage reference (pin 7) with a resistor (R5). The medium voltage reference must be well decoupled by a capacitor (C27). The input impedance of the AD converter is given by R5 in parallel with Zin.



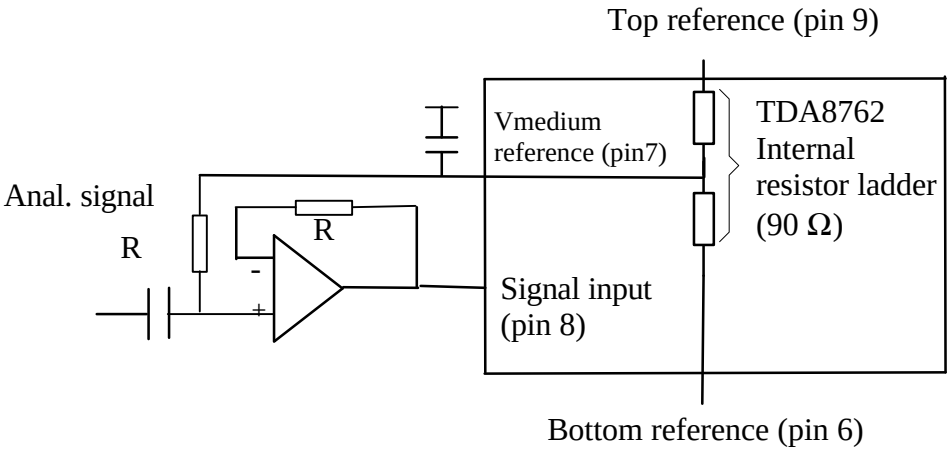
This method gives good results in the following domains: high common mode supply rejection (because both the voltage references and the input offset are derived from the same supply), very low noise level and low cost.
R5*C27 product must be high enough in order to avoid a coupling between the input signal and the medium reference. (C27=4.7µF for example) The offset on the input pin is: Vmed - (35µA*R5).

On board selection of the input offset, provided by the medium reference, is allowed by the J4.3 & J4.2 connection. In this case R5 and C27 must be soldered (SMD 1206 series solder prints).

6.3 INPUT OFFSET PROVIDED BY AN OPERATIONAL AMPLIFIER

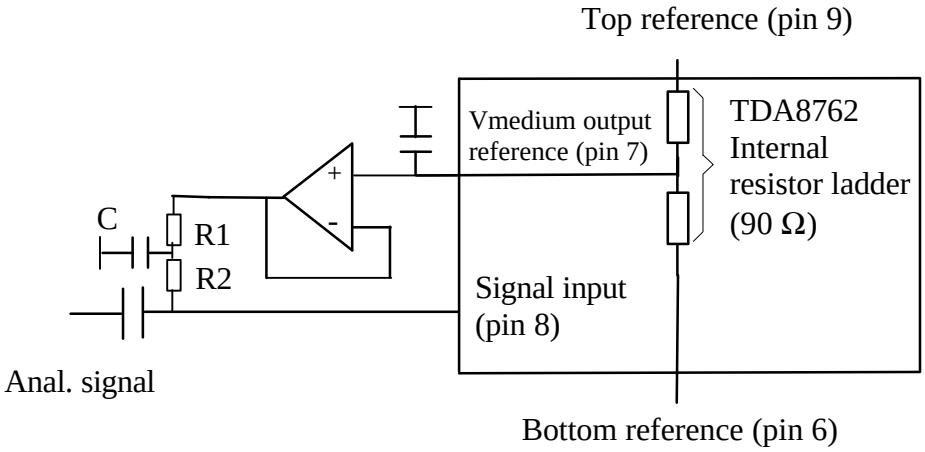
The middle output reference voltage and a low input offset operational amplifier can be used to provide an accurate input offset. Several methods can be used :

1°)



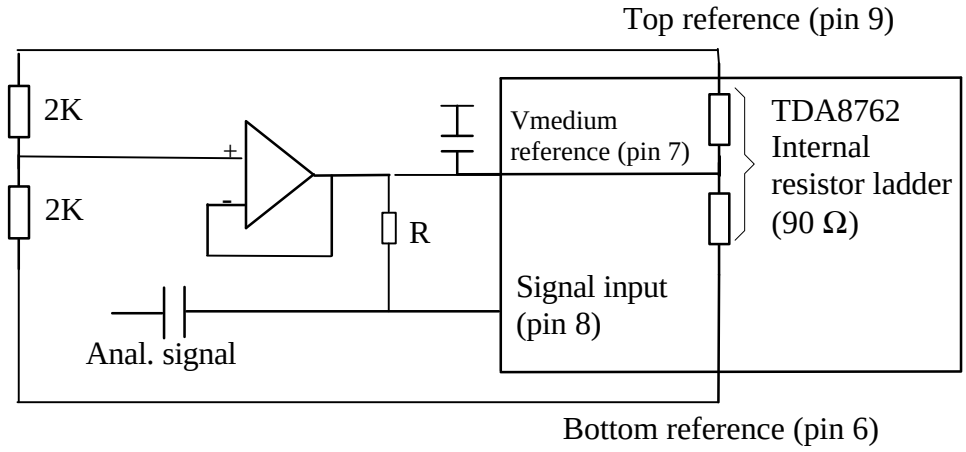
The R resistor in the op-amp loop compensates the offset due to the R resistor connected to Vmed. (R=1kΩ; C=1µF)

2°)



The amplifier does not need a high bandwidth, but the necessary time to load the C capacitor at ‘power on’ depends on the op.amp maximum output current. The input impedance is R2 // Zin. Zin is the ADC input impedance.

3°)



Medium reference is derived from top and bottom reference (input impedance is R // Zin).

7. CLOCK

7.1 CLOCK INPUT

The TDA8762 clock input (pin 1) is made up of a long pair tail ; therefore a low level AC clock input is allowed.

The clock input threshold is fixed at 1.3V. Consequently the DC component of the clock must be adjusted around 1.3V.
Also, the threshold value makes the TDA8762 compatible with TTL levels.

7.2 CLOCK JITTER

If the clock jitter and the slope of the analog input signal are high, sampling errors can appear.
Example :

The equation of a sinewave signal is **s(t)=A/2 sin(2 p F t)**,
where **A** is the ADC full scale amplitude (**A=1024 LSB**) and **F** is the sinewave frequency.
The slope of this signal is given by:
ds(t)/dt=A/2 2 p F cos(2 p F t)
this slope is maximum when t=0 (input voltage level is around middle code 511/512):
ds(0)/dt=A p F Volt/second.
That means that the middle code is available at the ADC input only during:
Tlsb=LSB/(A p F)=(1024 p F)$^{-1}$ second.
If the full scale sinewave frequency is **F = 10 Mhz**, then **Tlsb = 31 ps**
Consequently the clock jitter must be lower than this value.
If a 20 Mhz full scale sinewave is sampling, the jitter must be lower than 15 ps.

Remarks :

If the sample clock frequency and the input signal frequency have the same jitter (or phase noise), the sampling error due to jitter can be avoided.
Consequently it is not suitable to do precise dynamic measurements of the ADC characteristics with the on board quartz oscillator, except if the input signal frequency and the quartz oscillator frequency are correleted.

8. ADC SUPPLIES

All the ADC supplies VCCA (pin 3), VCCD (pin 11), VCCO1 (pin 13), VCCO2 (pin 28) are derived from the on board 7805 regulator and are well decoupled from each other by the means of LC filters.

VCCA stands for TDA8762 analog parts supply.
VCCD stands for TDA8762 digital internal parts supply.
VCCO1, VCCO2, stand for TDA8762 digital output buffers supplies.

Normally all the supplies are fixed around 5V and the differences between supplies must stay in the range of -0.25V to +0.25V (-0.4 to +0.4 for VCCA-VCCO and VCCD-VCCO).
In some cases (low voltage logic output interface, see section 9) it may be interesting to decrease the value of VCCO1 & VCCO2. This is allowed on the demo-board with the the J2 connector.

9. DIGITAL OUTPUTS / LOW VOLTAGE LOGIC COMPATIBILITY

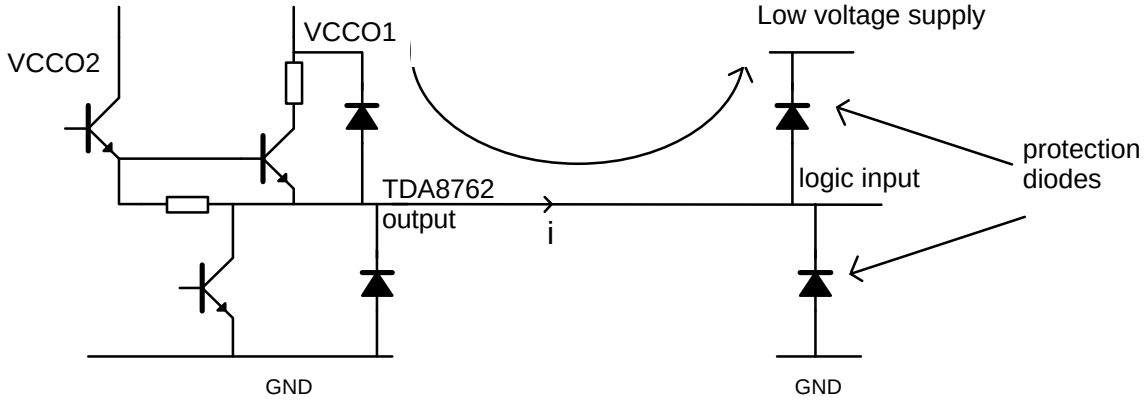
There are different kinds of low voltage logic (Philips low voltage CMOS & BiCMOS logic, LV, LVC, HLL,...) but generally direct connection of 3V logic inputs on the TDA8762 outputs is allowed. For general information about 3V and 5V logic compatibility refer to the AN240 application note included in the IC23 Philips databook.

A direct connection of the TDA8762 outputs with LVC family inputs is allowed because the LVC has no protection diodes on its inputs.

In other cases, one should pay attention to the digital device input structure.

The maximum TDA8762 high output voltage level is normally VCCO1-0,75V (with a high resistive load). Usually this value is never reached in dynamic mode because it should last several µs.

When this value is reached (i.e. in static mode) the output current of the TDA8762 is limited by a resistor. Consequently if there is a protection diode between the digital input
and the voltage supply of the logic device, a small current will flow from the TDA8762 supply (VCCO1,VCCO2) to the low voltage supply though the TDA8762 output circuitry and the low voltage logic input protection diode (see schema):



This can happened if a LV logic family is used. The following measurements are obtained with a CMOS low voltage logic family (Philips 74LV04) and they show the current flowing through the protection diode of one input pin:

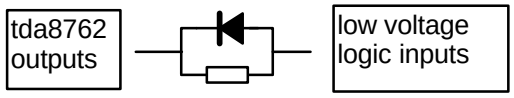
VCCO1, (V)	Low voltage supply (V)	i, max high level current (µA)	max high level (V)
5.25	3	180	3.8
5	3	140	3.77
4.75	3	70	3.74
5.25	3.3	120	4.07
5	3.3	55	4.04
4.75	3.3	15	3.97

Measured on 1 piece (typical value)

If currents in the protection diodes of the digital IC or if higher input voltage levels than the low voltage supply are prohibited, one or a combination of the following actions can be tried:

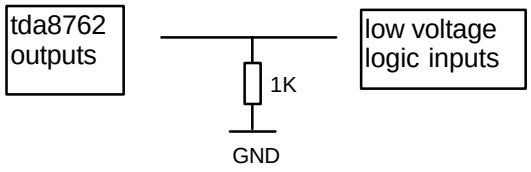
→ VCCO1 & VCCO2 can be decrease by adding a small resistor between power supply and VCCO1 & VCCO2. But VCCO1 & VCCO2 must stay higher than 4.5 V and the difference between VCCA or VCCD and VCCO1 and VCCO2 must stay below 500 mV. Usually a 17 Ohms resistor is suitable. With 4.5V for VCCO (this means 5V max. for VCCA and VCCD) the maximum TDA8762 high output level is 3.75 V (with a high resistive load).

→ Put a simple parallel resistor diode network in serie with the TDA8762 outputs:



The resistor reduces the high level current but it increases the falling time. So an additional diode allows a faster high to low transition.

→ Put a 1K pull-down resistor. This will keep the max high output level below 3V but it dramatically increases the current consumption.



→ It is also possible to put a pull-up resistor between TDA8762 outputs and the low power supply.

10. 10 BIT D/A CONVERTER

A 10 bit 5V supply/TTL input DAC (IC1) allows **rough** ADC evaluation with a scope or a spectrum analyzer. Analog output level is in the range of 3 to 5 volts.
The performances of the D/A converter are not as high as those of the A/D converter.
Consequently the on-board D/A converter cannot be use for a correct study of the ADC characteristics.

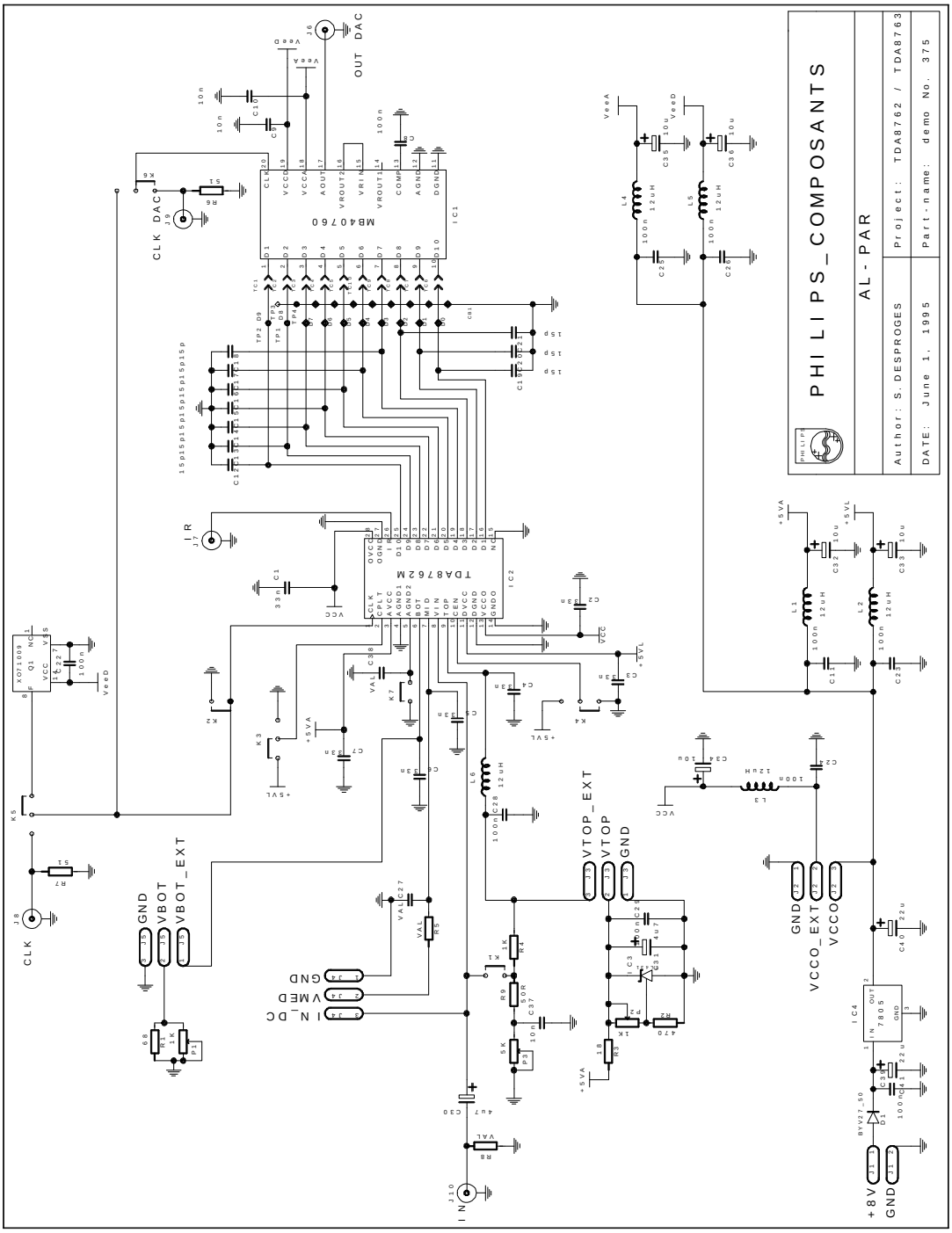
WARNING:

This D/A converter does not support low output loads, so it is necessary to check the strobe/scope input impedance before connection to the load.

11. DEMO BOARD DOCUMENTATION ELECTRIC DIAGRAM, COMPONENT LIST & PLACE

11.1 ELECTRIC DIAGRAM

(see next page)


PHILIPS_COMPOSANTS
AL - PAR
Author: S.DESPROGES
Project: TDA8762 / TDA8763
DATE: June 1, 1995
Part-name: demo No. 375
OUT DAC
CLK DAC
MB40760
TDA8762M
CLK
VTOP_EXT
VTOP
GND
VBOT
VBOT_EXT
I_N_DC
VMED
VCCO_EXT
VCCO
+8V
GND
IN

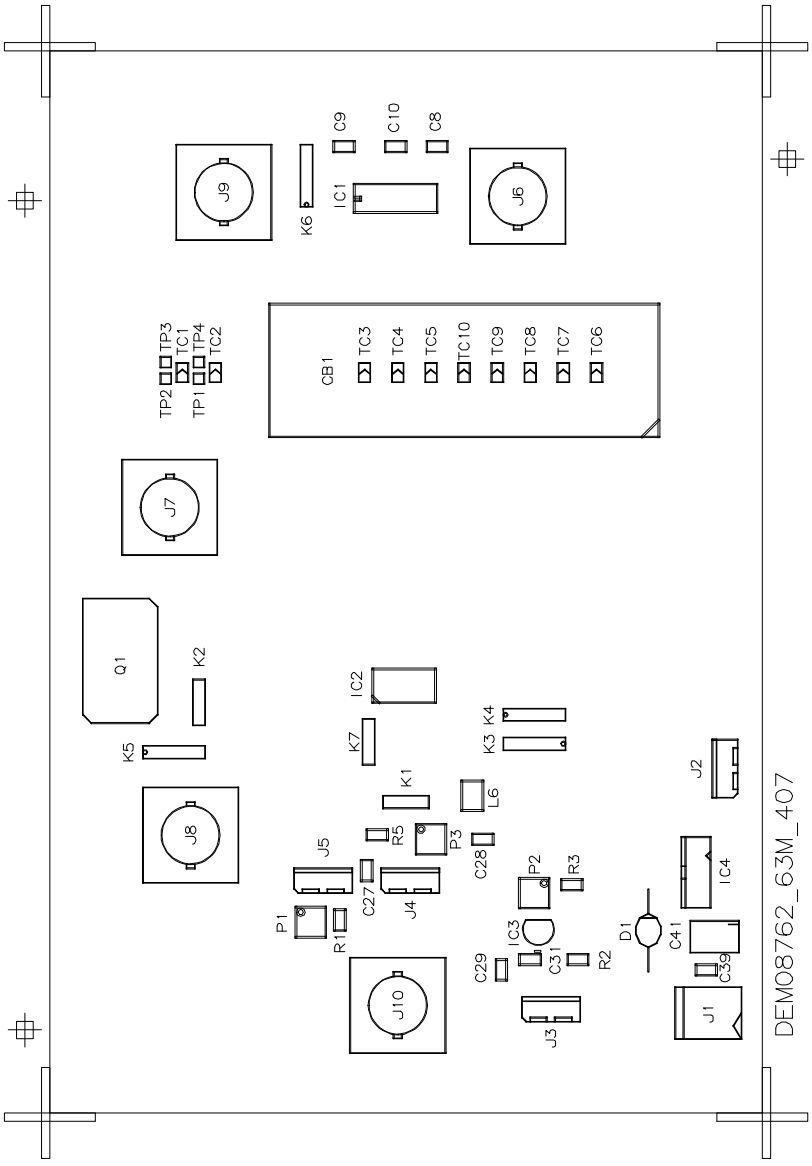
11.2 COMPONENT LIST

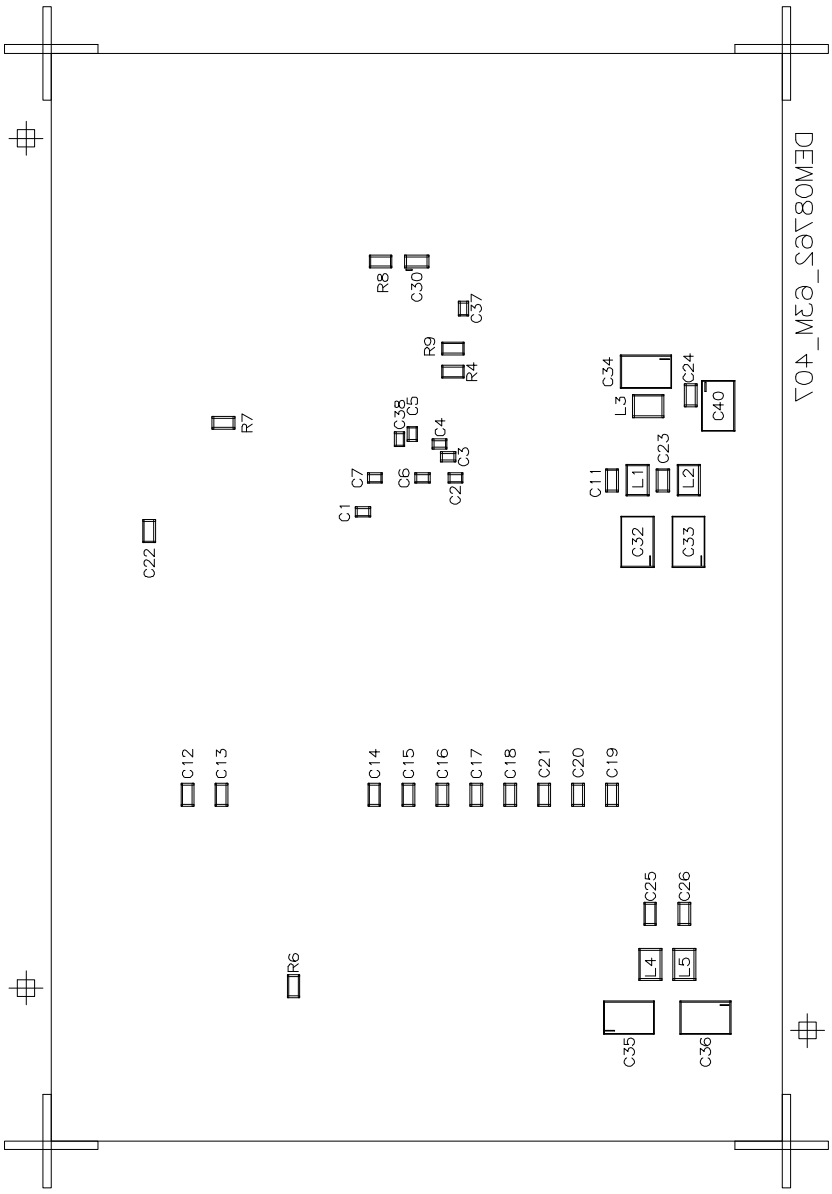
Reference	Value	Component
C1	33N	C0805
C2	33N	C0805
C3	33N	C0805
C4	33N	C0805
C5	33N	C0805
C6	33N	C0805
C7	33N	C0805
C8	100N	C1206
C9	10N	C1206
C10	10N	C1206
C11	100N	C1206
C12	15P	C1206
C13	15P	C1206
C14	15P	C1206
C15	15P	C1206
C16	15P	C1206
C17	15P	C1206
C18	15P	C1206
C19	15P	C1206
C20	15P	C1206
C21	15P	C1206
C22	100N	C1206
C23	100N	C1206
C24	100N	C1206
C25	100N	C1206
C26	100N	C1206
C27	VAL	C1206
C28	100N	C1206
C29	100N	C1206
C30	4U7	SPRAGUE_595D_A

Reference	Value	Component
C32	22U	SPRAGUE_293D_D
C33	22U	SPRAGUE_293D_D
C34	22U	SPRAGUE_293D_D
C35	22U	SPRAGUE_293D_D
C36	22U	SPRAGUE_293D_D
C37	10N	C0805
C38	VAL	C0805
C39	100N	C1206
C40	22U	SPRAGUE_293D_D
C41	22U	SPRAGUE_293D_D
CB1		8 BITS CONNECTOR (LSBs)
D1		BYV27_50
IC1		MB40760
IC2		TDA8762T
IC3		TL431
J1		CONN353MV2
J2		CONN1X3V_FCON
J3		CONN1X3V_FCON
J4		CONN1X3V_FCON
J5		CONN1X3V_FCON
J6		BNC
J7		BNC
J8		BNC
J9		BNC
J10		BNC
K1		2 POINT JUMPER
K2		2 POINT JUMPER
K3		SWITCH
K4		SWITCH
K5		SWITCH
K6		SWITCH

Reference	Value	Component
K7		2 POINT JUMPER
L1	12UH	LQH4N
L3	12UH	LQH4N
L4	12UH	LQH4N
L5	12UH	LQH4N
L6	12UH	LQH4N
P1	1K	3224W
P2	1K	3224W
P3	5K	3224W
Q1	20 up to 80MHz	X071009
R1	68	RMR01
R2	470	RMR01
R3	18	RMR01
R4	1K	RMR01
R5	VAL	RMR01
R6	51	RMR01
R7	51	RMR01
R8	VAL	RMR01
R9	50	RMR01
TC1-TC10		SOLDER POINTS
TP1-TP4		Test points 2 bits connector (MSBs)

11.3 COMPONENT PLACE




DEM08762_63M_407
R8
C30
C37
R9
R4
C34
C24
C40
L3
C38
C5
R7
C4
C3
C23
C7
C6
C2
C11
L1
L2
C1
C22
C32
C33
C12
C13
C14
C15
C16
C17
C18
C21
C20
C19
C25
C26
R6
L4
L5
C35
C36